What is claimed is:

1. A semiconductor memory device, comprising:

a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate;

an interlayer insulating layer formed over the semiconductor substrate;

a plug formed in the interlayer insulating layer, wherein the plug comprises a diffusion barrier layer and a seed layer for a electro plating;

a lower electrode of capacitor contacted to the seed layer;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer.

2. The semiconductor device as recited in claim 1, wherein the seed layer is selected from a group consisting of Ru layer, Ir layer, Pt layer, SrO layer, W layer, Mo layer, Co layer, Ni layer, Au layer and Ag layer.

3. The semiconductor device as recited in claim 1, wherein the diffusion barrier layer is selected from a group consisting of TiN layer, TiSiN layer, TiAlN layer, TaSiN layer, TaAlN layer, $IrO_2$ layer and $RuO_2$ layer.

4. The semiconductor device as recited in claim 1, further comprising a polysilicon layer between the diffusion barrier layer and the semiconductor substrate.

5. The semiconductor device as recited in claim 1, further comprising an ohmic contact layer between the diffusion barrier layer and the semiconductor substrate.

6. The semiconductor device as recited in claim 5, further comprising a polysilicon layer between the ohmic contact layer and the semiconductor substrate.

7. A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer to form a contact hole;

forming a plug in the contact hole, wherein the plug comprises a diffusion barrier layer and a seed layer for a electro plating;

forming a lower electrode of a capacitor contacted to the seed layer by using an electro plating technique;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

8. The method as recited in claim 7, wherein the seed layer is formed with Ru, Ir, Pt, SrO, W, Mo, Co, Ni, Au or Ag.

9. The method as recited in claim 8, the step of providing the semiconductor substrate comprising:

forming a conducting layer on the semiconductor substrate, wherein the conducting layer plays an electrode in the step of forming the lower electrode of the capacitor.

10. The method as recited in claim 8, wherein the diffusion barrier layer is formed with TiN, TiSiN, TiAlN, TaSiN, TaAlN, $IrO_2$ or $RuO_2$.

11. The method as recited in claim 8, wherein the dielectric layer is formed with $BaSrTiO_3$ layer, and wherein the upper electrode is formed with Pt layer, Ru layer or Ir layer.

12. A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and

wherein source/drain junctions are formed in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer to form a contact hole;

forming a plug in the contact hole, wherein the plug comprises a diffusion barrier layer and a seed layer for a electro plating;

forming a glue layer on the seed layer and the interlayer insulating layer;

forming a sacrificial layer on glue layer;

etching the sacrificial layer and the glue layer to form an opening defining a region of a lower electrode of a capacitor;

forming the lower electrode on the seed layer in the opening, by using an electro plating technique;

removing the sacrificial layer and the glue layer;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

13. The method as recited in claim 12, the step of forming the plug including:

forming the diffusion barrier layer in the contact hole;

etching the diffusion barrier to remove a part of the

diffusion barrier layer in the contact hole; and

forming the seed layer on the diffusion barrier layer.

14. The method as recited in claim 13, the step of providing the semiconductor substrate incluing:

forming a conducting layer on the semiconductor substrate, wherein the conducting layer plays an electrode in the step of forming the lower electrode.

15. The method as recited in claim 13, wherein the seed layer is formed with Ru, Ir, Pt, SrO, W, Mo, Co, Ni, Au or Ag, and wherein the diffusion barrier layer is formed with TiN, TiSiN, TiAlN, TaSiN, TaAlN, $IrO_2$ or $RuO_2$.

16. The method as recited in claim 15, wherein a silicon oxide layer and a nitride layer are staked to form the interlayer insulating layer.

17. The method as recited in claim 16, wherein the diffusion barrier layer is etched with a mixed gas comprising $Cl_2$ and $BCl_3$.

18. The method as recited in claim 16, the dielectric layer is formed with a $BaSrTiO_3$ layer, and wherein the upper electrode is formed with Pt layer, Ru layer or Ir layer.